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Marinescu, M.-C.V.; Rinard, M.;

[System Synthesis, 2001. Proceedings. The 14th International Symposium on](#)
2001 Page(s):215 - 220[AbstractPlus](#) | Full Text: [PDF\(576 KB\)](#) [IEEE CNF](#)[Rights and Permissions](#) 2. **A 32 kbyte integrated cache memory**Sawada, K.; Sakurai, T.; Nogami, K.; Shirotori, T.; Takayanagi, T.; Iizuka, T.; Maeda, T.; Matsunaga, M.; Maeguchi, K.; Kobayashi, K.; Ando, T.; Hayakashi, Y.; Miyoshi, A.; Sato, K.; [Solid-State Circuits, IEEE Journal of](#)
Volume 24, Issue 4, Aug. 1989 Page(s):881 - 888
Digital Object Identifier 10.1109/4.34065[AbstractPlus](#) | Full Text: [PDF\(640 KB\)](#) [IEEE JNL](#)[Rights and Permissions](#) 3. **A Broadband Packet Switch for Integrated Transport**

Hui, J.; Arthurs, E.;

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Volume 5, Issue 8, Oct 1987 Page(s):1264 - 1273[AbstractPlus](#) | Full Text: [PDF\(968 KB\)](#) [IEEE JNL](#)[Rights and Permissions](#) 4. **Distributed Microarchitectural Protocols in the TRIPS Prototype Processor**Sankaralingam, K.; Nagarajan, R.; McDonald, R.; Desikan, R.; Drolia, S.; Govindan, M.S.; Gratz, P. H.; Changkyu Kim; Liu, H.; Ranganathan, N.; Sethumadhavan, S.; Sharif, S.; Shivakumar, P.; Keck, M.; [Microarchitecture, 2006. MICRO-39. 39th Annual IEEE/ACM International Symposium on](#)
Dec. 2006 Page(s):480 - 491
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